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ARTICLE

Ferroelectric Field-Effect Transistors Based on MoS_2 and $CuInP_2S_6$ Two-Dimensional van der Waals Heterostructure

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Supporting Information

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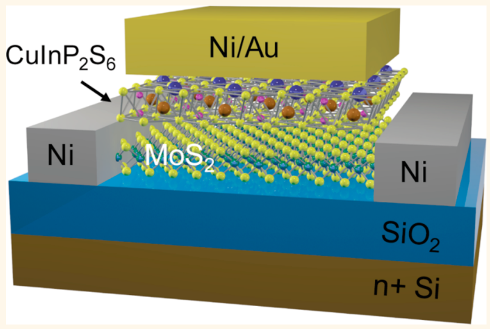
ABSTRACT: We demonstrate room-temperature ferroelectric field-effect transistors (Fe-FETs) with MoS_2 and $CuInP_2S_6$ two-dimensional (2D) van der Waals heterostructure. The ferroelectric $CuInP_2S_6$ is a 2D ferroelectric insulator, integrated on top of MoS_2 channel providing a 2D/2D semiconductor/insulator interface without dangling bonds. The MoS_2- and $CuInP_2S_6$-based 2D van der Waals heterostructure Fe-FETs exhibit a clear counterclockwise hysteresis loop in transfer characteristics, demonstrating their ferroelectric properties. This stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS_2 transistors because of the tuning of capacitance matching between the MoS_2 channel and the ferroelectric $CuInP_2S_6$, leading to the enhancement of the on/off current ratio. Meanwhile, the $CuInP_2S_6$ thin film also shows resistive switching characteristics with more than four orders of on/off ratio between low- and high-resistance states, which is also promising for resistive random-access memory applications.



KEYWORDS: MoS_2, $CuInP_2S_6$, 2D heterostructure, ferroelectric, field-effect transistors, resistive switching

Two-dimensional (2D) semiconductors, such as transition metal dichalcogenides (TMDs), have been extensively explored as channel materials for future electronic device applications because their atomically thin channels offer ideal electrostatic control to enhance the immunity to short channel effects. Molybdenum disulfide (MoS_2) has been widely studied in recent years as a promising channel material because of its ambient stability, appropriate band gap, and moderate mobility.[1−6] Inserting a ferroelectric insulator (such as hafnium zirconium oxide and lead zirconate titanate) into the gate stack of a metal-oxide-semiconductor field-effect transistor (MOSFET) as a ferroelectric field-effect transistor (Fe-FET) and negative capacitance field-effect transistor (NC-FET) has been widely studied for nonvolatile memory and low-power logic applications.[7−20] The integration of ferroelectric insulators and 2D semiconductor materials as 2D Fe-FETs[7−14] and 2D NC-FETs[15−20] has been proposed and studied to combine the advantages of both 2D semiconductors and ferroelectric-gated FETs. However, the nonideal 3D ferroelectric insulator/2D semiconductor interface leads to interface traps which degrade the device performance, variability, and reliability. The lack of dangling bonds on the surface of 2D materials also makes the atomic layer deposition (ALD) process of ferroelectric insulators difficult.[21] How to integrate an ALD ferroelectric insulator (*i.e.*, hafnium zirconium oxide) as a top-gate dielectric on 2D materials remains a challenge. The integration of 2D ferroelectric insulators together with 2D semiconductors as 2D van der Waals (vdW) heterostructures can be a potential solution to eliminate the interface issue, reduce the interface trap density, and achieve high-performance Fe-FETs. However, 2D ferroelectric material is rather rare because ferroelectricity tends to disappear on very thin films and requires breaking of the structural centrosymmetry.[22,23] A few 2D materials have been studied theoretically[23−26] and experimentally[27−30] that show ferroelectricity. The choice of a proper 2D ferroelectric insulator to integrate with 2D semiconductors is crucial because 2D vdW heterostructure Fe-FETs require a low leakage current gate insulator and room-temperature ferroelectricity for real device applications. Among these materials, $CuInP_2S_6$ (CIPS) has been recently explored as a room-temperature 2D ferroelectric material with switchable polarization down to ∼4 nm and low leakage current, which can be a promising candidate for 2D vdW heterostructure Fe-FETs.[29−32]

In this work, we synthesize the bulk CIPS crystal and examine the ferroelectricity of the 2D CIPS thin film by

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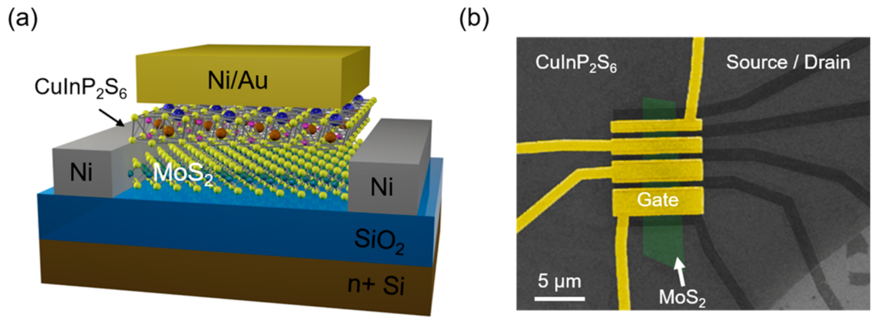

Figure 1. (a) Schematic view of a MoS_2/CIPS 2D heterostructure Fe-FET. Few-layer MoS_2 is applied as the channel material. Fifteen nanometer Ni is used as the source/drain electrodes. The back-gate stack includes heavily n-doped Si as the gate electrode and 300 nm SiO_2 as the gate dielectric. The top-gate stack consists of CIPS as the ferroelectric gate insulator and Ni/Au as the gate electrode. (b) Top-view false-color SEM image of fabricated MoS_2/CIPS 2D heterostructure Fe-FETs with different channel lengths, capturing Ni/Au top-gate electrodes, Ni source/drain electrodes, CIPS ferroelectric gate insulators, and MoS_2 channels.

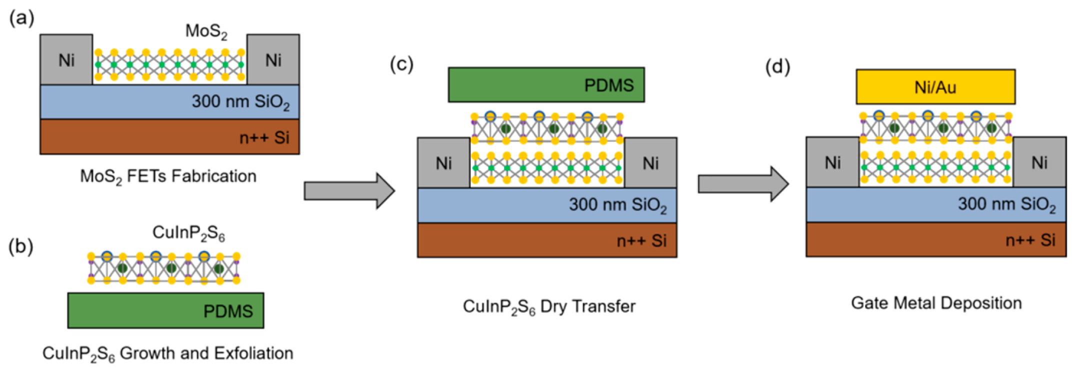

Figure 2. Fabrication process of MoS_2/CIPS 2D heterostructure Fe-FETs. (a) MoS_2 FET fabrication. (b) $CuInP_2S_6$ growth and exfoliation. (c) $CuInP_2S_6$ dry transfer. (d) Gate metal deposition.

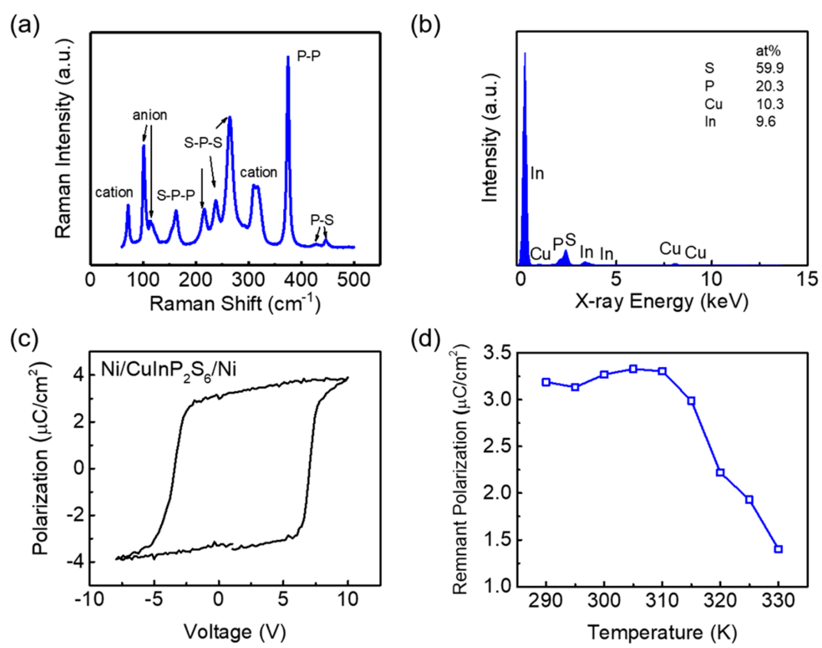

Figure 3. (a) Raman spectrum of exfoliated CIPS thin film at room temperature. (b) EDS spectrum of exfoliated CIPS thin film. The atomic percent (atom %) of S, P, Cu, and In is 59.9, 20.3, 10.3, and 9.6, respectively. EDS analysis shows almost perfect $CuInP_2S_6$ stoichiometry. (c) Polarization−voltage measurement at 290 K on ferroelectric CIPS MIM capacitor (Ni/0.6 μm CIPS/Ni). (d) Temperature dependence of remnant polarization on the CIPS thin film measured using the same capacitor as in (c), suggesting a ferroelectric Curie point at ~315 K.

electrical polarization−voltage (P−V) measurement. We demonstrate MoS_2/CIPS 2D vdW heterostructure Fe-FETs at room temperature. The ferroelectric CIPS is integrated on top of the MoS_2 channel as a ferroelectric insulator, which offers a 2D/2D semiconductor/insulator interface. The MoS_2/CIPS 2D vdW heterostructure Fe-FETs exhibit a clear

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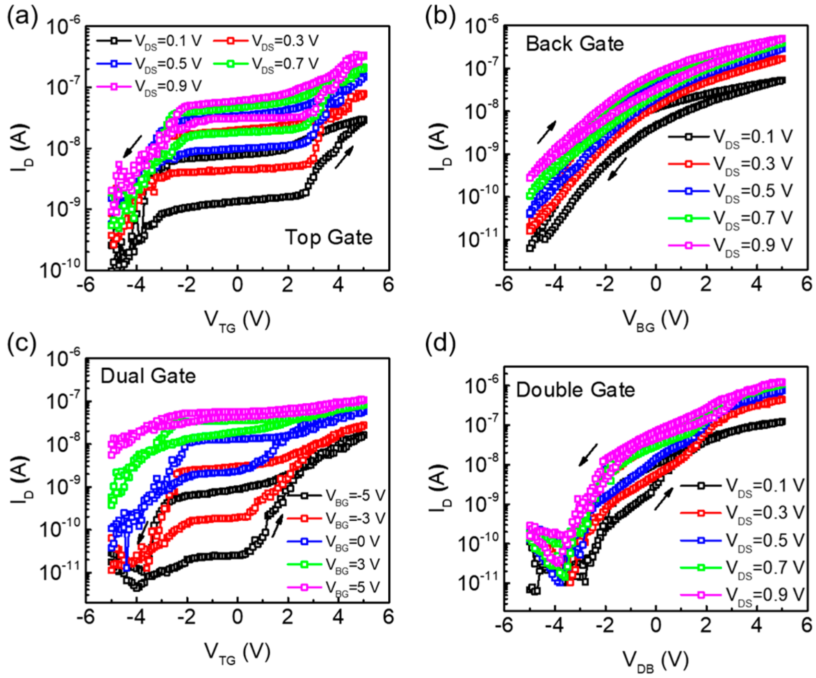

Figure 4. (a) Top-gate I_D-V_{GS} characteristics of a MoS_2/CIPS 2D heterostructure Fe-FET measured at room temperature with a floating back-gate. The device has a channel length of 1 μm and channel width of 2.1 μm. The thickness of the MoS_2 flake is about 7 nm, and the thickness of the CIPS thin film is about 0.4 μm. (a) Back-gate I_D-V_{GS} characteristics measured at room temperature with a floating top-gate, using the same MoS_2/CIPS 2D heterostructure Fe-FET as in (a). (c) Top-gate I_D-V_{GS} characteristics at V_{DS} = 0.1 V and at various V_{BG} measured at room temperature, using the same MoS_2/CIPS 2D heterostructure Fe-FET as in (a). (d) I_D-V_{GS} characteristics with the same V_{TG} and V_{BG} measured at room temperature, using the same MoS_2/CIPS 2D heterostructure Fe-FET as in (a).

counterclockwise hysteresis loop in transfer characteristics, demonstrating their ferroelectric properties. Meanwhile, this stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS_2 transistors because of the tuning of capacitance matching between the MoS_2 channel and the ferroelectric $CuInP_2S_6$, which leads to the enhancement of the on/off current ratio. Meanwhile, the resistive switching characteristics of CIPS are also studied, and more than four orders of on/off ratio between low- and high-resistance states are realized.

RESULTS AND DISCUSSION

The schematic view of a MoS_2/CIPS 2D heterostructure Fe-FET is shown in Figure 1a. The device consists of few-layer MoS_2 as the channel material, a few hundred nanometer CIPS as the ferroelectric gate insulator for a top-gate Fe-FET, a 300 nm SiO_2 as the back-gate insulator, and heavily doped silicon substrate as the back-gate electrode. The 40 nm Ni/50 nm Au is used as top-gate electrode, and 15 nm Ni is used as source/drain electrodes. The device has a dual-gate structure, in which the MoS_2 channel can be controlled by both top-gate and back-gate. A top-view false-color scanning electron microscopy (SEM) image of several fabricated devices with different channel lengths (L_{ch}) is shown in Figure 1b, capturing Ni/Au top-gate electrodes, Ni source/drain electrodes, CIPS ferroelectric gate insulators, and MoS_2 channels. The detailed fabrication process is shown in Figure 2, and detailed information can be found in the Methods section.

Figure 3a illustrates the Raman spectrum of an exfoliated CIPS thin film at room temperature, showing the same characteristics as those reported in bulk CIPS crystals at ferroelectric phase.[33] Cation (Cu^{I}, In^{III}) and anion ($P_2S_6^{4-}$) vibrations are responsible for peaks in the 50−80, 90−140, and 300−320 cm^{-1} ranges. Multiple peaks between 140 and 290 cm^{-1} are caused by S−P−P and S−P−S modes, and the peak at 380 cm^{-1} corresponds to P−P stretching. The 410−460 cm^{-1} peaks correspond to P−S oscillations. Figure 3b shows the energy-dispersive spectroscopy (EDS) spectrum of the exfoliated CIPS thin film. The atomic percent (atom %) of S, P, Cu, and In is 59.9, 20.3, 10.3, and 9.6, respectively. EDS analysis shows near perfect $CuInP_2S_6$ stoichiometry. The CIPS thin film samples used in Raman and EDS measurement were mechanically exfoliated from a bulk CIPS crystal (the synthesis of the bulk CIPS crystal is discussed in Supporting Information section 1) onto a silicon substrate with 300 nm thermally grown SiO_2. The atomic structure illustration of CIPS is shown in Supporting Information section 2. It contains an ABC sulfur stacking filled by Cu, In, and a P−P pair. The non-centrosymmetric structure leads to spontaneous polarization and ferroelectricity at temperatures below the Curie point.[31] To study the ferroelectric properties of the CIPS thin film, metal−insulator−metal (MIM, Ni/CIPS/Ni) capacitors are fabricated as a test structure. The $P-V$ characteristics are measured from 290 to 330 K. Figure 3c shows the $P-V$ measurement at 290 K on a CIPS MIM capacitor with a CIPS thickness (T_{FE}) of ~0.6 μm. The $P-V$ characteristic of CIPS shows a clear ferroelectric hysteresis loop with 3.2 $\mu C/cm^2$ remnant polarization (P_r) and 8.9 × 10^{-3} V/nm coercive field (E_c). Note that the success in $P-V$ measurement of the CIPS MIM capacitor suggests that the leakage current through CIPS is sufficiently low, which indicates CIPS can be a good candidate as a ferroelectric gate insulator for Fe-FETs and NC-FETs. Figure 3d shows the temperature-dependent remnant polarization of CIPS extracted from the $P-V$ measurement of the same device as in Figure 3c from 290 to 330 K. The P_r of

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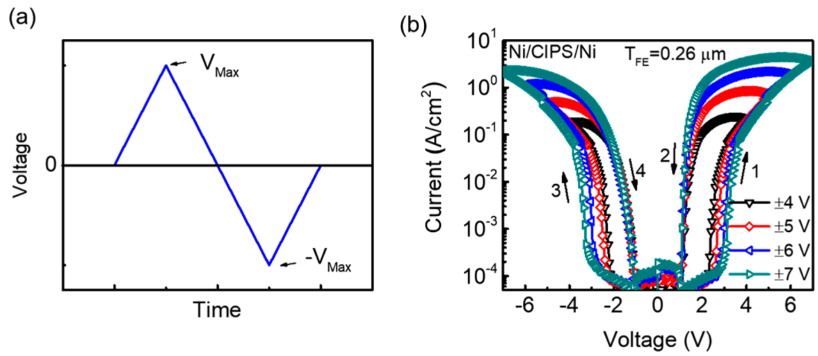

Figure 5. (a) Illustration of $I-V$ measurement on the ferroelectric CIPS MIM capacitors. The voltage across the MIM capacitor was first swept from 0 V to a positive V_{Max} and then to a negative $-V_{Max}$ and back to 0 V. (b) $I-V$ characteristics at different sweep ranges of a ferroelectric CIPS MIM capacitor with a CIPS thickness of about 0.26 μm at room temperature, showing ferroelectric resistive switching with more than four orders of on/off ratio between low- and high-resistance states.

CIPS starts to drop rapidly at about 315 K, suggesting that the Curie point of ferroelectric to paraelectric phase transition is about 315 K. The detailed temperature-dependent $P-V$ measurements can be found in Supporting Information section 4.

Figure 4 shows the electrical characterization of a MoS_2/CIPS 2D vdW heterostructure Fe-FET at room temperature. The device has a channel length of 1 μm and channel width of 2.1 μm. The thickness of the MoS_2 flake (T_{ch}) is about 7 nm, and the thickness of CIPS thin film is about 0.4 μm. Figure 4a shows the I_D-V_{GS} characteristics measured using the top-gate (0.4 μm CIPS as ferroelectric gate insulator) with the back-gate floating at top-gate voltage (V_{TG}) from −5 to 5 V and at drain-to-source voltage (V_{DS}) from 0.1 to 0.9 V. The gate leakage current is smaller than drain current at all different gate voltages, so that the leakage current through CIPS does not have impact on the I_D-V_{GS} characteristics. The simultaneously measured gate leakage current can be found in Supporting Information section 3. The transfer characteristics show a clear ferroelectric hysteresis loop (counterclockwise) at all V_{DS}. A larger on/off ratio between the low- and high-resistance state can be observed at lower V_{DS}. Figure 4b shows the I_D-V_{GS} characteristics measured using the back-gate (300 nm SiO_2 as gate insulator) with the top-gate floating at back-gate voltage (V_{BG}) from −5 to 5 V and at V_{DS} from 0.1 to 0.9 V. The transfer characteristics show a clockwise hysteresis loop, which is common in MoS_2 MOSFETs and is induced by charge trapping at the SiO_2/MoS_2 interface and in bulk SiO_2. The characteristics have minor changes of top-gate or bottom-gate being grounded instead of floating, showing the two gates' capacitance coupling has a minor effect on each other. Figure 4c shows the I_D-V_{GS} characteristics measured using the top-gate (0.4 μm CIPS as gate insulator) at V_{DS} = 0.1 V with different V_{BG} from −5 to 5 V. The ferroelectric hysteresis loop in the I_D-V_{GS} characteristics is found to be modulated by the back-gate bias, as shown in Figure 4c. With more negative V_{BG}, a larger hysteresis loop can be observed, which suggests that back-gate bias can be used to modulate the on/off current ratio of the MoS_2/CIPS 2D vdW heterostructure Fe-FETs for better memory performance. The origin of the modulation of the ferroelectric hysteresis loop comes from the capacitance matching between the capacitance of CIPS (C_{FE}) and the semiconductor capacitance (C_S) of the MoS_2 channel. For a ferroelectric-gated FET, it is already known that because of the negative capacitance effect of the ferroelectric material, if $|C_{FE}| < C_S$, the ferroelectric-gated FET is a Fe-FET with hysteresis, whereas if $|C_{FE}| > C_S$, the ferroelectric-gated FET is a NC-FET without hysteresis if parasitic capacitance is negligible.[19] A detailed analysis on the value of $|C_{FE}|$ and C_S is discussed in Supporting Information section 6. Therefore, as the back-gate voltage can affect the electrostatics in the MoS_2 channel and also tune the C_S, the back-gate bias can modulate the capacitance matching between C_{FE} and C_S, so that the ferroelectric hysteresis loop can be modulated. It also indicates that this dual-gate structure enables the electrically controllable reconfiguration of the devices as either logic devices or memory devices by applying proper back-gate voltage. Figure 4d shows the I_D-V_{GS} characteristics measured using the same V_{TG} and V_{BG} at V_{DS} from 0.1 to 0.9 V, which is simply the result of impact from both gates.

Except for the ferroelectricity in the CIPS thin film and its applications in Fe-FETs, the CIPS with a MIM capacitor structure also shows resistive switching characteristics which can be used in nonvolatile resistive random-access memory (ReRAM) applications, as shown in the Figure 5. Figure 5a illustrates the $I-V$ measurement process on the MIM capacitors. The voltage across the capacitor was first swept from 0 V to a positive maximum voltage (V_{Max}) then to a negative $-V_{Max}$ and then back to 0 V. Figure 5b shows the $I-V$ characteristics with different gate voltage sweep ranges (V_{Max} from 4 to 7 V) of a CIPS MIM capacitor with T_{FE} = 0.26 μm, measured at room temperature, showing ferroelectric resistive switching with more than four orders of on/off ratio between low- and high-resistance states. The resistive switching between the low- and high-resistance states originates from the ferroelectric polarization switching, which leads to the change of band alignment between metal and CIPS.[34] The detailed band diagrams in different polarization states are discussed in Supporting Information section 7. The resistive switching characteristics of the CIPS are also affected by V_{Max}. A larger V_{Max} leads to a smaller on-resistance but a larger voltage to reset to high-resistance state, as shown in Figure 5b, which can enable multiple design rooms. These results suggest that CIPS is a promising 2D material for nonvolatile ReRAM applications also.

CONCLUSION

In summary, MoS_2/CIPS 2D vdW heterostructure Fe-FETs at room temperature are demonstrated. The ferroelectric CIPS is integrated on top of the MoS_2 channel as a ferroelectric

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insulator, which offers a 2D/2D semiconductor/insulator interface. The MoS_2/CIPS 2D vdW heterostructure Fe-FETs exhibit a stable ferroelectric hysteresis loop in transfer characteristics. Meanwhile, this stable nonvolatile memory property can also be modulated by the back-gate bias of the MoS_2 transistors because of the tuning of capacitance matching between the MoS_2 channel and the ferroelectric $CuInP_2S_6$, leading to the enhancement of the on/off current ratio. Meanwhile, the resistive switching characteristics of CIPS are also studied, with more than four orders of on/off ratio between low- and high-resistance states demonstrated.

METHODS

$CuInP_2S_6$ Growth. Single-crystal CIPS were grown by solid-state reaction based on previous works.[32] The detailed growth process can be found in Supporting Information section 1.

Device Fabrication. MoS_2 was transferred onto a 300 nm SiO_2/Si substrate using Scotch tape exfoliation. Fifteen nanometer Ni was deposited by electron-beam evaporation, followed by a lift-off process as a MoS_2 back-gate transistor. The procedure to transfer CIPS on top of MoS_2 is based on a dry transfer process.[35] CIPS was first mechanically exfoliated onto a polydimethylsiloxane (PDMS) substrate. Then the PDMS/CIPS film was stamped on top of the MoS_2 channel. The PDMS film was then removed mechanically because of the stronger adhesion between CIPS and the substrate. Another 40 nm Ni and 50 nm Au were then deposited by electron-beam evaporation and realized by a lift-off process.

Device Characterization. The thickness of the CIPS was measured using a Veeco Dimension 3100 atomic force microscope system. SEM and EDS analysis were done using a Hitachi S-4800 FE-SEM and an Oxford X-Max silicon drift detector. Electrical characterization was carried out with a Keysight B1500 system with a Cascade Summit probe station. P−V measurement was done using a Radiant RT66C ferroelectric tester. Raman measurements were carried out on a HORIBA LabRAM HR800 Raman spectrometer.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b01810.

Additional details for CIPS growth and structures, gate leakage current, temperature-dependent P−V and I−V measurement, Landau coefficients extraction, and band diagrams of CIPS-resistive switching mechanism (PDF)

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Author Contributions

M.S. and P.-Y.L. contributed equally to this work. P.D.Y. conceived the idea and supervised the experiments. P.-Y.L. synthesized the $CuInP_2S_6$. M.S. and P.-Y.L did the device fabrication, electrical measurement, and analysis. G.Q. did the Raman spectrum measurement. Y.D. conducted EDS analysis. M.S., P.-Y.L, and P.D.Y. cowrote the manuscript, and all authors commented on it.

Notes

The authors declare no competing financial interest.

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